**Synapses with homo/hetero-synaptic plasticity enabled by ferroelectric polarization modulated Schottky diodes**

**Andreas Grenmyr1,2, Jiayuan Zhang1,2, Fengben Xi1, Stefan Wiefels3, Detlev Grützmacher1,4, Qing-Tai Zhao1**

1Peter Grünberg Institute (PGI-9), Forschungszentrum Jülich, 52428 Jülich, Germany

2 Faculty of Electrical Engineering and Information Technology, RWTH Aachen University, 52074 Aachen, Germany

3Peter Grünberg Institute (PGI-7), Forschungszentrum Jülich, 52428 Jülich, Germany

4Peter Grünberg Institute (PGI-10), Forschungszentrum Jülich, 52428 Jülich, Germany

**Summary.** Several recently proposed synapses suffer from limited linearity or constrained means of weight adjustment, which can be overcome by incorporating additional modulating terminals. In this study, we explore the use of ferroelectric Schottky transistors (FE-SBFETs) with either a single or dual gate, which exhibit excellent linearity and demonstrate the potential of the second gate terminal for modulation. The incorporation of multiple gates can enable more sophisticated control of the synapse, resulting in greater flexibility for tuning the synaptic weight. The demonstrated high linearity is critical for precise and accurate weight adjustment, as it allows for a larger number of distinguishable conductive states. Therefore, the incorporation of multiple gates and input terminals represents a promising direction for developing more versatile and high-performance neuromorphic devices.

 In recent years, there has been rapid progress in Artificial Intelligence. However, conventional methods rely on standard CMOS technology that suffers from high energy consumption and the Von Neumann Bottleneck, a limitation in data transfer capacity between processing and memory units [1][2]. These issues can be addressed by using neuromorphic devices that mimic the behavior of synapses and neurons in the human brain [2]. One such device is the ferroelectric field-effect transistor (FeFET). Nonetheless, many FeFETs are based on source and drain doping, creating either n-channel or p-channel FeFETs. The synaptic behavior is realized by the ferroelectric polarization modulated channel resistance. However, this device structure prevents ferroelectric polarization from controlling source/drain resistances, resulting in degraded linearity when applying potentiating or depressing pulses. As illustrated in Fig.1a, forming Schottky diodes at the drain and source can solve this problem and allows ferroelectric polarization to control all three resistances, improving linearity, as shown in our previous work [3]. This device can be further improved. Fig. 1b shows a dual top gate that adds a fourth terminal, enabling heterosynaptic behavior where the fourth terminal acts as a modulatory neuron that can impact the synapse's behavior [4].

Figure 1. Illustration of FE-SBFET structures of: a) three terminals, and b) four terminal devices with dual-gate. The second gate can be used as a modulatory neuron.

Figure 2 displays the long-term potentiation/depression (LTP/LTD) results obtained from both 3-terminal (Fig. 2a) and 4-terminal (Fig. 2b, c) devices. In the homosynaptic device with 3-terminals (Fig. 2a), we applied 50 potentiating pulses with an amplitude of -0.7V. The increasing domain polarization resulting from the pulses creates more holes in the channel, reducing source, drain, and channel resistances. This is followed by 50 depressing pulses with an amplitude of 0.5V for depression. As explained previously, the combination of Schottky diodes and channel modulation enables the creation of more conductive states (in this case, 50 states) and high linearity of the devices.

 In the 4-terminal devices, voltage pulses are applied to the programming gate on the source side, and the modulation of the synaptic characteristics by the modulatory neuron enables heterosynaptic plasticity. The impact of the input voltage at the fourth terminal, VMOD, is clearly visible in Fig. 2b-c. At VMOD = -1V, applied to the gate at the drain side, the conductive states have higher current and lower variance noise than those at VMOD=0 V. This can be explained by the modulation of the drain contact, which affects the overall drain current. The advantage of heterosynaptic plasticity is the reduction of positive feedback compared to homosynaptic plasticity, which increases the controllability for potentiation or depression of the synapses [5].

Figure 2. a) Measured LTP/LTD results for the homosynaptic 3-terminal device, 50/50 potentiating/depressing pulses are applied. b) and c): For the heterosynaptic 4-terminal device, the modulating voltage influences the conductive states. For a modulating gate voltage VMOD= -1V the conductivity of the weight states increases, and the noise decreases compared to VMOD= -1V.



Furthermore, the additional fourth terminal offers an advantage of logic gates for in-memory computing [1]. As shown in Fig. 3, if only one of VMOD and VPRO is negative, the current is very low. However, if both are negative at the same time, the current becomes high, enabling the implementation of the AND function using only a single device. The ability to use the same device and process for both in-memory computing and as a synapse simplifies the integration of neuromorphic systems. Therefore, the synaptic device with Schottky diodes and heterosynaptic behavior is a promising candidate for a building block in neuromorphic computing systems. In-memory computing and synaptic functionality are crucial components of such systems and combining them into a single device can lead to more efficient and compact systems.

Figure 3. Logic AND function implemented by using a single heterosynaptic device.

Acknowledgements

This work was partially supported by the Federal Ministry of Education and Research (BMBF, Germany) in the project NEUROTEC (16ME0398K).

# References

[1] G. Pedretti and D. Ielmini, *Electron.*, vol. 10, no. 9, 2021

[2] S. H. Jo, T. Chang, et al., *Nano Lett.*, vol. 10, no. 4, pp. 1297–1301, 2010

[3] F. Xi *et al.*, *ACS Appl. Mater. Interfaces*, vol. 13, no. 27, 2021

[4] F. Xi *et al.*, *Adv. Electron. Mater.*, 2022

[5] M. Chistiakova, et al, *Neuroscientist*, vol. 20, no. 5, 2014.